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Sir:

Under the provisions of 35 USC 119 and 37 CFR 1.55(a), the applicant hereby claims the right of priority based on the following application(s):

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NORWAY	20003508	07/07/00

A certified copy of the above-noted application(s) is(are) attached hereto.

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Title of the invention: Addressing of memory matrix

ADDRESSING OF MEMORY MATRIX

A 1. Introduction.

The present invention concerns pulsing protocols for the addressing of individual crossing points in passive matrices used for data storage and display purposes, where a major goal is to avoid disturbing non-addressed crossing points in the same matrices. Another major goal is to minimize the cumulative signal from non-addressed cells in such matrices during reading of stored data. Applications typically involve, but are not limited to, matrices containing a ferroelectric thin film that acts as non-volatile memory material.

A 2. Prior art.

Passive matrix addressing implies the use of two sets of parallel electrodes that cross each other, typically in orthogonal fashion, creating a matrix of crossing points that can be individually accessed electrically by selective excitation of the appropriate electrodes from the edge of the matrix. Advantages of this arrangement include simplicity of manufacture and high density of crossing points, provided the functionality of the matrix device can be achieved via the two-terminal connections available at each crossing point. Of particular interest in the present context are display and memory applications involving matrices where the electrodes at each crossing point sandwich a material in a capacitor-like structure, henceforth termed a "cell", and where the material in the cells exhibits polarizability and hysteresis. The latter property confers non-volatility on the devices, i.e. they exhibit a memory effect in the absence of an applied external field. By application of a potential difference between the two electrodes in a given cell, the material in the cell is subjected to an electric field which evokes a polarization response, the direction and magnitude of which may be thus set and left in a desired state, representing e.g. a logic "0" or "1" in a memory application or a brightness level in a display application. Likewise, the polarization status in a given cell may be altered or deduced by renewed application of voltages to the two electrodes addressing that cell.

Examples of passive matrix devices employing ferroelectric memory substances can be found in the literature dating back 40-50 years. Thus, W.J. Merz and J.R. Anderson described a barium titanate based memory device in 1955 (W.R. Merz and J.R. Anderson, "Ferroelectric storage devices", Bell.Lab.Record. 1 335-342 (1955)), and similar work was also reported by others promptly thereafter (See, e.g. C.F. Pulvari "Ferroelectrics and their memory applications" IRE Transactions CP-3 3-11 (1956), and D.S. Campbell "Barium titanate and its use as a memory store", J. Brit. IRE 17 (7) 385-395 (1957)). An example of a passive matrix addressed display rendered non-volatile by a ferroelectric material can be found in US Pat. 3,725,899 by W. Greubel, filed in 1970.

In view of its long history and apparent advantages, it is remarkable that the passive matrix addressing principle in conjunction with ferroelectrics has not had a greater impact technologically and commercially. While important reasons for this may be traced back to the lack of ferroelectric materials that satisfy the full range (technical and commercial) of minimum requirements for the devices in question, a major factor has been certain inherent

negative attributes of passive matrix addressing. Prominent among these is the problem of disturbing non-addressed crossing points. The phenomenon is well recognized and extensively discussed in the literature, both for displays and in memory arrays. Thus, the basics shall not be discussed here, but the reader is referred to, e.g.: A. Sobel: "Some constraints on the operation of matrix displays" IEEE Trans.Electron Devices (Corresp.) ED-18 797 (1971), and L.E.Tannas Jr.: "Flat panel displays and CRTs", pp.106 et seq., (Van Nostrand 1985). Depending on the type of device in question, different criteria for avoiding or reducing disturbance of non-addressed crossing points can be defined. Generally, it is sought to lower the sensitivity of each cell in the matrix to small-signal disturbances, which can be achieved by cells that exhibit a nonlinear voltage-current response, involving e.g. thresholding, rectification and/or various forms of hysteresis.

Although general applicability is claimed for the present invention, particular focus shall be directed towards ferroelectric memories, where a thin film of ferroelectric material is stimulated at the matrix crossing points, exhibiting a hysteresis curve as illustrated generically in Fig.1. Typically, writing of a bit is accomplished by applying a voltage differential across the film at a crossing point, causing the ferroelectric to polarize or switch polarization. Reading is analogously achieved by applying a voltage of a given polarization, which either causes the polarization to remain unchanged after removal of the voltage or to flip to the opposite direction. In the former case, a small current will flow in response to the applied voltage, while in the latter case the polarization change causes a current pulse of magnitude larger than a predefined threshold level. A crossing point may arbitrarily be defined as representing a "0" bit in the former case, a "1" bit in the latter.

A material with hysteresis curve as shown in Fig.1 will change its net polarization direction upon application of a field that exceeds E_c. However, partial switching shall take place upon application of voltages below this value, to an extent depending on the material in question. Thus, in a matrix with a large number of crossing points, repeated stimuli of non-addressed crossing points may ultimately degrade the polarization states in the matrix to the point where erroneous reading results. The amount and type of stimulus received by non-addressed crossing points in a cross-bar passive matrix during write and read operations depends on how the voltages are managed on all addressing lines in the matrix during these operations, henceforth termed the "pulsing protocol". The choice of pulsing protocol depends on a number of factors, and different schemes have been proposed in the literature, for applications involving memory materials exhibiting hysteresis. Examples of prior art shall now be given.

In US Pat.2,942,239, J.P. Eckert, Jr. et al. describe pulsing protocols for memory arrays with magnetic cores, each with a magnetic hysteresis curve analogous to the ferroelectric one shown in Fig.1. Although claiming general applicability for memory elements exhibiting bistable states of remanent polarization, including ferroelectrics, their invention contains only specific teachings on magnetic data storage where separate contributions to the total magnetic flux in each cell are added or subtracted from several independent lines intersecting in each cell. This is reflected in how cells are linked up in the proffered embodiments, with a readout protocol providing superposition of a slow, or "background" biasing stimulus being applied to all or a subset (e.g. a column or a row) of the cells in the matrix, and with a fast selection pulse being applied between the crossing lines containing the addressed cell. No teachings are given on efficient voltage protocols for two-terminal, capacitor-like memory cells combining high speed, random access to data with restoration of the destructively read information.

In,US Pat. 3,002,182, J.R.Anderson describes the problem of polarization loss by partial switching of ferroelectric memory cells in passive matrix addressed arrays of ferroelectric-filled capacitors. To reduce the partial switching polarization loss during writing, he teaches the use of simultaneous application of addressing pulses to an addressed row and column such that the former executes an electrical potential swing of typically $+2V_s/3$ to $+3V_s/4$ (where V_s is the nominal switching voltage) while the latter swings to a negative value sufficient for the potential difference between the electrodes at the selected crossing point to reach the value V_s. With the remaining columns being switched to a potential in the range $+V_s/3$ to $+ V_s/4$, only the selected cell in the matrix receives a significant switching field, and partial switching at the other crossing points is strongly reduced (the reduction depends on the material properties of the ferroelectric, in particular the shape of the hysteresis curve and the magnitude of the dielectric constant). In an alternative pulsing scheme, he teaches the application of additional "disturbance compensating pulses" subsequent to each writing operation, where the selected row is clamped at zero potential while the selected and non-selected columns are pulsed to $+ V_s/4$ to $+ V_s/3$ and $-V_s/4$ to $-V_s/3$, respectively. The latter operation is claimed to reduce the partial switching induced loss of polarization even further. No physical explanation was provided for this choice of pulsing scheme, however, which appears to rely to a large degree on the inventor's empirical experience with the ferroelectric materials of his day, in particular barium titanate. While the basic choice of polarities appear plausible and indeed intuitive to the person skilled in the art of ferroelectrics, the description given is insufficient to provide an adequate guide to selection of pulse magnitudes and timing in concrete terms for generalized cases. For reading out the stored information or clearing the cells before a writing operation, the inventor teaches the application of the full switching voltage $-V_s$ to the selected row or rows, referring to "a manner well known in the art". Selection of the column electrode voltages is treated in a nebulous fashion. It may appear that the selected column electrode is clamped at ground, with all non-selected column electrodes biased to $- V_s/3$ or $- V_s/4$ (cf. Fig.4B in US Pat. 3,002,182). However, this leads to a voltage load of $2V_s/3$ to $3V_s/4$ on the non-selected cells in the same row as the selected cell, with obvious danger of partial switching. Thus, it would at best seem that the invention shall be poorly suited for situations where a large number of read operations are involved between each write, and the general applicability to realistic ferroelectric devices appears doubtful.

In US Pat. 3,859,642, J. Mar describes a memory concept based on a passive matrix addressing scheme, where an array of capacitors with programmable bistable capacitance values is subjected to a two-level excitation during the reading cycle. The memory function resides in the bistability of the capacitors, which are assumed to be of the metal-insulator-semiconductor (MIS) type or equivalent, exhibiting a hysteresis loop which is centered around an offset voltage and well removed from the zero offset point. Writing of data is achieved by biasing the row and column lines crossing at the selected capacitor to polarities +V and –V, respectively, alternatively to –V and +V, respectively, depending on which of the two bistable states is to be written. The resulting net bias is thus +-2V on the selected capacitor, and does not exceed an absolute magnitude V on non-selected capacitors, where V is defined as being below threshold for writing. Partial writing is apparently not considered to be a problem, and no particular provisions are described in that connection beyond the simple scheme referred here. Thus, the teachings of US Pat. 3,859,642 can not be seen as having any prior art significance relative to the subject matter of the present invention.

L.E. Tannas, Jr. describes a one-third selection scheme for addressing a ferroelectric matrix arrangement in US Pat. 4,169,258. In this case, the x- and y lines in a passive matrix addressing arrangement are subjected to a pulsing protocol where (unipolar) voltages with

relative magnitudes 0, 1/3, 2/3 and 1 are applied in a coordinated fashion to all x- and y-lines. Here, voltage value 1 is the nominal voltage amplitude employed for driving a given cell from a logic state "OFF" to "ON", or *vice versa*, with the typical coercive voltage being exemplified as a value between 1/2 and 2/3. An important limitation of the scheme taught in that patent is that the pulse protocols are predicated upon all cells starting out with the same initial polarization magnitude and direction ("OFF"), i.e. the whole matrix must be blanked to an "OFF" state before a new pattern of states can be written into the matrix cells. Furthermore, any "ON" state on the same y-line as the addressed cell shall receive a disturb pulse of magnitude 2/3 in the direction of the "OFF" state, leading to partial switching in most known ferroelectrics. While these limitations may be acceptable in certain types of displays and memories, this is not the case in the vast majority of applications.

Total blanking is not subsumed under what Tannas Jr. terms the conventional method "one-half selection scheme", which is described in detail in the quoted patent US Pat. 4,169,258. However, the latter scheme exposes the non-selected cells to disturbing pulses of relative value ½. This is generally deemed unacceptable for all practical memory applications employing traditional ferroelectric materials such as inorganic ceramics. Furthermore, the one-half selection scheme is only described in terms of single switching events in the addressed cells, which destroy the pre-switching polarization states.

Thus, in memory and display applications where it is desired to be able to change the logic content of individual cells without disturbing other cells or having to blank and reset the whole device, there is a clear need for improvement over the existing prior art.

A 3. The object(s) of the invention.

It is a major object of the invention to describe voltage vs. time protocols for driving the x- and y passive matrix addressing lines in non-volatile memories exhibiting ferroelectric-like hysteresis curves so as to minimize disturbance of non-selected memory cells during writing as well as reading of data to/from said memories. It is a further object of the invention to describe voltage protocols that reduce charging/discharging transients and thus to achieve high speed. It is a further object of the invention to describe voltage protocols that permit simple, reliable and cheap electronic circuitry to perform drive and sense operations on the memory matrices.

A 4. The realisation of the object(s) of the invention.

The key to realizing the object(s) of the invention is to control the time dependent voltages on all the x- and y-lines in the matrix in a coordinated fashion according to one of the protocols described hereunder. Said protocols ensure that no non-addressed cell (crossing point) in the matrix experiences an interline voltage exceeding a predetermined value which is well below a level at which disturbance or partial switching occurs. The basic principles and explicit examples shall now be decribed with reference to the appended figures, where:

A 5. List of drawing figures.

Fig.1 shows a principle drawing of a hysteresis curve for a ferroelectric memory material.

Fig.2 is a principle drawing of a passive matrix addressing arrangement with crossing electrode lines, and cells containing a ferroelectric material localized between these electrodes where they overlap. For easy reference and to conform with standard usage, we shall henceforth refer to the horizontal (row) and vertical (column) lines as "bit lines" (abbreviated: BL) and "wordlines" (abbreviated: WL), respectively, as indicated in the figure.

Fig.3 illustrates the sum of voltage steps around a closed loop in the matrix.

Fig.4 shows a read and write voltage protocol requiring three separate voltage levels to be controlled on the word- and bit lines.

Fig.5 shows an alternative variant of the three level voltage protocol in Fig.4.

Fig.6. shows a read and write voltage protocol requiring four separate voltage levels to be controlled on the word- and bit lines.

Fig.7 shows an alternative variant of the four level voltage protocol in Fig.6.

Fig.8. shows a read and write voltage protocol requiring five separate voltage levels to be controlled on the word- and bit lines.

Fig.9 shows an alternative variant of the five level voltage protocol in Fig.8.

Figures 10 - 13 show alternative voltage protocols to those shown in figures 6-9, the difference being that pre-charging pulses on inactive word lines are now included.

Fig.14 shows an example of a read and write protocol involving a pre-read reference cycle.

Fig.15 shows a readout scheme based on full row parallel detection.

B 1. Examples of embodiments/reduction to practice.

It is understood that the materials constituting the memory function in displays and memory devices as per the instant invention exhibit hysteresis as exemplified in a generic fashion in Fig.1. Relevant materials are electrets, ferroelectrics or a combination of the two. For simplicity, it shall be assumed in the following that the material in question is a ferroelectric, but this shall not restrict the generality of the present invention.

As a consequence of prior exposure to electric fields, the material is assumed to reside in one of two polarization states when in zero external field, represented by the points $+P_R$ and $-P_R$ in Fig.1. Application of a voltage across the cell containing the ferroelectric causes the latter to change its polarization state, tracing the hystersis curve in a manner well known to the person skilled in the art of ferroelectrics. For convenience, the hysteresis curve in Fig.1 is shown with the voltage rather than the field along the abscissa axis.

Below shall be described how, in a passive matrix configuration, voltages can be applied to the crossing word- and bit lines in such a fashion that a single, freely chosen cell in the matrix experiences a potential difference V_S between the two electrodes crossing at that point which has sufficient magnitude to cause the ferroelectric to switch its polarization direction in either positive or negative direction (depending on the polarity of the applied field between the electrodes) and ending up at one of the points $+P_R$ or $-P_R$ on the hysteresis curve after removal of the externally imposed field. At the same time, no other cell in the matrix shall be subjected to a potential difference that causes an unacceptable (according to prior defined criteria) change in the polarization state. This is ensured by the potential difference across non-addressed cells (the "disturbing voltage") never exceeding $+-V_S/n$, where n is an integer or non-integer number of typical value of 2 or more.

Depending on the required switching speed, etc, the nominal switching voltage V_S employed for driving the polarization state of the ferroelectric is typically selected considerably larger than the coercive voltage V_C (cf. Fig.1). However, it cannot be chosen arbitrarily large, since the pulsing protocols described here shall only reduce the disturbing voltage to a certain fraction (typically 1/3) of V_S, which level should be less than V_C.

Before proceeding to a discussion of specific pulsing protocols, it may be useful to view the problem in a generalized fashion. Referring to the matrix shown in Fig.2: It is desired to apply a voltage that is sufficiently high to switch a given cell, either for defining a given polarization direction in that cell (writing), or for monitoring the discharge response (reading). Accordingly, the cell is selected by setting the potentials of the associated word- and bit lines (the "active" lines) such that:

$$(1) \qquad \Phi_{activeBL} - \Phi_{activeWL} = V_S .$$

At the same time, the numerous word- and bit lines that cross at non-addressed cells must be controlled in potential such that the disturbing voltages at these cells are kept below the threshold for partial switching. Each of these "inactive" word- and bit lines cross the active bit- and word line at a non-addressed cell. Referring to Fig.2, one notes that 4 distinct classes of cells can be defined in the matrix, according to the perceived voltages across the cells:

i) $V_i = \Phi_{activeBL} - \Phi_{activeWL}$: Active word line crossing active bit line (the selected cell)
ii) $V_{ii} = \Phi_{inactiveBL} - \Phi_{activeWL}$: Active word line crossing inactive bit line,
iii) $V_{iii} = \Phi_{activeBL} - \Phi_{inactiveWL}$: Inactive word line crossing active bit line,
iv) $V_{iv} = \Phi_{inactiveBL} - \Phi_{inactiveWL}$: Inactive word line crossing inactive bit line.

In practical devices where it is desired to minimize cost and complexity, it is of primary interest to focus on the special case where all inactive word lines are at a common potential $\Phi_{inactiveWL}$, and correspondingly all inactive bit lines are at a common potential $\Phi_{inactiveBL}$. By summing voltages around a closed loop in the matrix grid as shown in Fig.3, the following condition applies:

$$(2) \qquad V_i = V_{ii} + V_{iii} - V_{iv} .$$

Given the value of $V_i = V_S$, the minimum voltage value attainable across the non-addressed cells is thus:

$$(3) \qquad |V_{ii}| = |V_{iii}| = |V_{iv}| = V_S/3.$$

To achieve this, at least 4 separate potentials (i.e. Φ_0 , $\Phi_0+V_S/3$, $\Phi_0+2V_S/3$, Φ_0+V_S; where Φ_0 is a reference potential) must be imposed on the electrodes in the matrix, and any change in potential on one of the electrodes must be coordinated with adjustments in the other potentials such that no cell experiences a voltage exceeding $V_s/3$. In practice, several other factors must be heeded also, e.g. related to minimizing switching transients (charge/discharge currents) and reducing the complexity of the driving circuitry, resulting in pulsing protocols such as those described below. One example is an overall shift in potentials by adding or subtracting the same voltage to all 4 levels.

B.1.1. 3 level ($V_S/2$) switching protocol.

In certain special cases, a simplified pulsing protocol may be used, where all inactive word and bit lines are given the same potential, i.e. $V_{iv} = 0$. In that case, the minimum voltage value attainable across non-addressed cells becomes:

$$(4) \qquad V_{ii} = V_{iii} = V_S/2$$

and at least 3 separate potentials are needed for managing the write and read operations (i.e. Φ_0 , $\Phi_0+V_S/2$, Φ_0+V_S; where Φ_0 is a reference potential).

As was mentioned above, partial switching may represent a serious problem at voltage levels of $V_S/2$, rendering 3 level protocols unacceptable. However, the degree of partial switching at a given applied voltage depends explicitly on the ferroelectric material in question. Referring to Fig.1, materials with a square shaped hysteresis curves shall in many applications yield acceptable performance.

Recently, certain classes of ferroelectrics such as organic polymers have received much attention as memory substances in advanced data storage concepts. In addition to other attractive features, theses materials exhibit hysteris curves far more square shaped than those of the ceramic ferroelectrics that have traditionally dominated developments in the field of ferroelectric-based non-volatile memory devices. Thus, it has become relevant to define pulsing protocols which can satisfy the requirements of realistic and optimized electronic device designs. Following upon the partial switching problems that discouraged development and exploitation of early efforts based on 3 level switching protocols, these aspects have received very little attention, which the present invention sets out to remedy.

Examples of preferred embodiments.

Figures 4 and 5 illustrate some 3 level pulsing protocols according to the present invention, comprising a complete read cycle and a refresh/write cycle. Only the pulse diagrams for the active word- and bit lines are shown. The inactive word lines may be kept stable at $V_S/2$ throughout the read/write cycle, as may the inactive bit lines. Alternatively, the latter may during the read cycle each be connected with a separate sense amplifier, which would be biased near the bit line voltage when the bit line clamp is released (full row readout). In the diagrams shown in Figures 4 and 5, the time markers are as follows:

t_0 : word line latched, active pulldown to 0 (Fig.4) or pullup to V_S (Fig.5).
t_1 : bit line clamp released – sense amp. On

- t_2 : bit line decision – data latched
- t_3 : word line returned to quiescent $V_S/2$
- t_4 : write data latched on bit lines
- t_5 : word line pulled to V_S (Fig.4) or 0 (Fig.5) - set/reset capacitors
- t_6 : word line returned to quiescent $V_s/2$
- t_7 : bit lines actively returned to V_S (fig.4) or 0 (Fig.5) clamp
- t_8 : read/write cycle complete

The read cycle investigates the state of the polarization of the addressed cell. Depending on the polarization direction, the read operation may leave the polarization unchanged, or it may reverse the polarization direction (destructive read). In the latter case, the information must be refreshed if it is desired avoid loss of stored data. This implies that the polarization must be driven in the opposite direction of the read operation in an appropriate cell (not necessarily the one that was read) somewhere in the matrix. This is achieved by the part of the protocol dedicated to refresh/write, as shown. The two branches in the bit line voltage protocol correspond to the cases where the polarization is left unchanged and reversed, respectively. An isolated write operation is trivially achieved by omitting the preceding read operation.

As shown in Figures 4 and 5, it is clear that non-addressed cells shall not receive voltages exceeding ½ of the nominal switching voltage, neither during reading or refresh/writing periods. In addition, one notes that there are included event delays in the pulsing sequence to facilitate transient ring-down and latching of data. Depending on how the memory device is to be operated, the bit line potential in the quiescent state (i.e. between read/refresh/write cycles) may be chosen to match that of the bit line at the start of the read cycle (cf. Figures 4 and 5) or it may match the quiescent potential of the word line (not shown here). In the former case, appropriate when cycling is intense and at high speed, charging currents at the start of the read cycle are minimized. In the latter case, long term effects of an imposed field in the cells (e.g. imprint) are avoided.

It should be clear that the examples shown in Figures 4 and 5 may be modified (e.g. by concurrent shifting of all potentials, or by minor departures from exact voltage levels in the 3 level scheme shown) without departing from the essential principles illustrated therein.

B.1.2. 4 level ($V_S/3$) switching protocol.

As described above, by employing at least 4 different potential levels on the word and bit lines, one can ensure that no non-addressed cell experiences a voltage exceeding 1/3 of the nominal switching voltage.

Examples of preferred embodiments.

Figures 6 and 7 illustrate two variants of a preferred scheme for reading as well as refreshing/writing data, according to the present invention. Here, the time markers are as follows:

- t_0 : quiescent state: all word- and bit lines at $2V_S/3$ (Fig.6) or $V_S/3$ (Fig.7)
- t_1 : inactive bit lines adjusted from quiescent value to $V_S/3$ (Fig.6) or $2V_S/3$ (Fig.7)
- t_2 : addressed bit line(s) adjusted to V_S (Fig.6) or 0 (Fig.7). Time delay from t_1 to t_2 is arbitrary; zero or negative timings are acceptable also

- t_3 : after a programmable read-setup delay, the addressed word line is adjusted from quiescent potential to 0 V (Fig.6) or V_S (Fig.7), inducing a voltage of magnitude V_S between addressed word- and bit lines. Unaddressed word lines remain at $2V_S/3$ (Fig.6) or $V_S/3$ (Fig.7)
- t_4 : addressed word line returned to quiescent potential after read delay
- t_5 : all bit lines returned to quiescent potential
- t_6 : read cycle now complete. All word- and bit lines in quiescent state ($2V_S/3$ in Fig.6; $V_S/3$ in Fig.7)
- t_7 : all inactive word lines adjusted from quiescent to $V_S/3$ (Fig.6) or $2V_S/3$ (Fig.7)
- t_8 : Fig.6: Addressed bit line(s) to be written to logic state "1" are adjusted to 0 V or are left at quiescent potential to remain in logic "0" .
  Fig.7: Addressed bit line(s) to be written to logic state "0" are adjusted to V_S or are left at quiescent potential to remain in logic "1"
- t_9 : addressed word line is adjusted to V_S (Fig.6) or 0 (Fig.7), introducing a voltage of magnitude V_S across addressed cell(s)
- t_{10} : addressed bit line(s) returned to quiescent $2V_S/3$ (Fig.6) or $V_S/3$ (Fig.7) after write delay
- t_{11} : all word lines returned to quiescent potential
- t_{12} : write cycle complete. All word- and bit lines in quiescent.

Apart from the increased voltage level complexity, the basic features are similar to those referred above in connection with the three level schemes. Now, however, no non-addressed cell is exposed to a voltage exceeding $V_S/3$ in the course of a complete read/write cycle, which shall cause only minor partial switching in most ferroelectric materials of relevance here. Again, several variants on a common theme are possible. Thus, Figs. 6 and 7 show a return to zero applied voltage across all cells in the quiescent state (cf. the above discussion under the 3 level switching protocol), which corresponds to word- and bit line potentials of $2V_S/3$ or $V_S/3$, whereas other potential levels on the word- and bit lines are possible in the quiescent state that either yield zero voltages across the cells or voltages of absolute value $\leq |V_S|/3$. Such variants shall be assumed obvious to the skilled person and shall not be pursued in further detail here.

The timing diagrams in Figs. 6 and 7 are equivalent in principle, one being an "inverted" version of the other. In practice, however, one may be preferred over the other. Thus, the scheme shown in Fig.6 implies a voltage at the sense amplifier input during the read cycle near V_S . In the scheme of Fig.7, however, the voltage is near zero. This may permit the use of low voltage components with a single high voltage pass transistor per bit line.

B.1.3. 5 level ($V_S/3$) switching protocol.

A class of seemingly more complex, but in certain respects more simply implemented pulsing protocols involve the application of 5 different potential levels to the word- and bit lines during a complete read/write cycle.

Examples of preferred embodiments.

Explicit examples of two preferred embodiments are shown in Figs. 8 and 9. The time markers are as follows:

t_0 : quiescent state: all word- and bit lines at $2V_S/3$ (Fig.6) or $V_S/3$ (Fig.7)
t_1 : inactive bit lines adjusted from quiescent value to $V_S/3$ (Fig.6) or $2V_S/3$ (Fig.7)
t_2 : addressed bit line(s) adjusted to V_S (Fig.6) or 0 (Fig.7). Time delay from t_1 to t_2 is arbitrary; zero or negative timings are acceptable also
t_3 : after a programmable read-setup delay, the addressed word line is adjusted from quiescent potential to 0 V (Fig.6) or V_S (Fig.7), inducing a voltage of magnitude V_S between addressed word- and bit lines. Unaddressed word lines remain at $2V_S/3$ (Fig.6) or $V_S/3$ (Fig.7)
t_4 : addressed word line returned to quiescent potential after read delay
t_5 : all bit lines returned to quiescent potential
t_6 : read cycle now complete. All word- and bit lines in quiescent state ($2V_S/3$ in Fig.6; $V_S/3$ in Fig.7)
t_7 : inactive bit lines adjusted from quiescent to V_S (Fig.8) or $V_S/3$ (Fig.9)
t_8 : Fig.8: Addressed bit line(s) to be written to the "1" state are adjusted to $V_S/3$, while those that shall remain in state"0" are adjusted to V_S.
Fig.9: Addressed bit line(s) to be written to the "0" state are adjusted to $V_S/3$, while those that shall remain in state"1" are adjusted to V_S.
t_9 : addressed word line is adjusted to $4V_S/3$ (Fig.8) or 0 (Fig.9), introducing a voltage of magnitude V_S across addressed cell(s). Non-addressed word lines remain at $2V_S/3$.
t_{10} : addressed word lines returned to quiescent potential after write delay
t_{11} : all bit lines returned to quiescent potential
t_{12} : write cycle complete. All word- and bit lines in quiescent.

Here, a fifth voltage level, V_{CC}, is involved. It is typically of magnitude $4V_S/3$, and is applied to the active word line during the reading (Fig.8) or refresh/write (Fig.9) cycle. One notes that while the 4 level schemes in Figs. 6 and 7 require all word- and bit lines to be driven at four levels in the course of the complete read/write cycle, the 5 level schemes in Figs. 8 and 9 require only 3 separate voltage levels to be applied to the word lines and 3 separate but not identical voltage levels to be applied to the bit lines. This provides opportunities for optimization and simplification of the driving and sensing electronics supporting the device. Further simplification can be realized by choosing $4V_S/3 = V_{CC}$ close to the power supply voltage.

B.1.4. Switching protocols involving pre-charging of non-addressed cells on active bit lines.

So far, primary focus has been on avoiding partial switching of non-addressed cells. However, it is also desirable to design switching protocols that simultaneously minimize the effect of parasitic current flows wihin the memory matrix during the read cycle:

In memory matrices based on passive matrix addressing, the areal data storage density is maximized by using matrices that are as large as possible. This implies that each matrix should contain the largest possible number of crossing points between word- and bit lines, and any given bit line must consequently cross a large number of word lines. When a given word- and bit line crossing is selected, the large number of non-selected crossing points between the bit line and all of the non-selected crossing word lines constitute a correspondingly large

number of parasitic current leakage paths (capacitive, inductive, ohmic) which may add up to slow down the device and reduce the contrast ratio of as-read logic "1"s and "0"s.

One method of reducing the effect of parasitic currents on the determination of logic states is to pre-charge the non-addressed cells on the active bit line to a level corresponding to that which would be approached during the reading of the active cell. This procedure is implicit in the voltage protocols shown in Figures 6-9: At time point 2, i.e. prior to applying the read voltage step to the active word line (at time point 3 in the figures) the active bit line voltage is shifted to its read cycle value, creating a voltage bias between the active bit line and all word lines. This initiates the spurious current flows in all the non-active cells on the active bit line. These currents are typically transient, reflecting polarization phenomena in the cells, and die out or are greatly diminished after a short time. Thus, by making the time gap between time points 2 and 3 sufficiently long, the spurious current contributions to the switching currents sensed during the reading cycle are greatly diminished. Certain limitations adhere to this scheme: If the time gap between time points 2 and 3 becomes very long, it has obvious implications on the data access speed and overall read cycle time. Aditionally, the cumulative effect of repeated cycling with long pre-charging times may be to cause partial switching and imprint, which was sought avoided by having zero voltage across all cells in the quiescent state.

The voltage protocol diagrams in Figs. 6-13 do not show the sense amplifier timing, which may vary from case to case, depending upon the dynamics of the polarization switching and spurious current response in the addressed and in the non-addressed cells. The sense amplifiers must be activated after time point 2 to avoid the spurious current transient from the non-addressed cells, and not much later than time point 3 in order to capture any polarization reversal current in active cells that are switched by the read cycle.

One notes that by advancing the time point 2 well ahead of time point 3, not only the inactive cells on the active bit line are subjected to an early voltage bias of magnitude $|V_S/3|$, but also the active cell. Thus, some of the switching charge in the active cell is drained away before the sense amplifier has been connected. The magnitude of this effect, which is undesirable since it reduces the read signal, depends on the polarization characteristics of the memory material in the cells and may range from negligible to significant. In the latter case, one may implement a slight modification of the voltage protocol by introducing a voltage shift on the inactive word lines as illustrated in Figures 10-13: The leading edge of the shift occurs at time point 0, and the trailing edge coincides with the leading edge of the active bit line voltage shift at time point 2. By precisely controlling the trailing and leading edge shifts at time point 2, the voltage across the non-addressed cells on the active bit line shall rise from zero to a magnitude $|V_S/3|$ at time point 0 and remain unchanged at this value until time point 5, i.e. after completion of the read cycle. The time point 2 may now be optimized for the readout process in the active cell, without limitations relating to driving the precharge transient in the non-addressed cells. As can be seen from Figures 10-13, the voltage across non-addressed cells is always maintained at less than a magnitude $|V_S/3|$ in these modified schemes, but 4 voltage levels are now involved on the word lines in the 5 level protocols, compared to 3 levels previously.

B.1.5. Switching protocols involving a reference pre-read cycle.

Another scheme for circumventing or alleviating the problems relating to parasitic currents in non-addressed cells on active bit lines shall now be described.

For concreteness, refer to, e.g. the 4 level timing diagram shown in Fig.6. The pre-charge scheme described in the above paragraphs implies that the active bit line has been shifted to its read cycle value at time point 2, and ensuing parasitic currents have been significantly reduced by the time the active word line is switched at time point 3. The logic state in the addressed cell is determined by the sense amplifier which records the charge flowing to the bit line during a defined time interval that starts near the time point 3 and stops before the time point 4.

Ideally, such pre-charge schemes shall enable detection of the charge flowing in response to the shifting of the active word line at time point 3, without interference from parasitic currents through cells at inactive word lines. In practice, the parasitic currents may die down slowly and/or have an ohmic (i.e. non-transitory) component such that some parasitic charge is captured by the sense amplifier. Although the magnitude of the parasitic current component flowing through each non-addressed cell on the active bit line may be small, the currents from hundreds or thousands of non-addressed cells on the active bit line may add up to become very significant, corrupting the readout results.

Assuming stable and predictable conditions, such a parasitic contribution may in principle be removed by subtracting a fixed amount of charge from that recorded by the sense amplifier during the reading cycle. In many instances, however, the magnitude and variability of the parasitic contribution makes this inappropriate. Thus, in addition to the manufacturing tolerances for the device, the fatigue and imprint history may vary within wide limits between different cells in the same memory device and even on the same bit line, and the parasitic current may depend strongly upon the device temperature at the time of read-out. In addition, the parasitic current associated with a given non-addressed cell on the active bit line may depend on which logic state it is in. In that case the cumulative parasitic current from all non-addressed cells on the active bit line shall depend on the set of data stored in those cells, which defies prediction.

In order to obtain a true measure of the cumulative parasitic currents in connection with a given read-out event, one may implement a pre-read reference cycle as exemplified in Fig.14: The pre-read cycle immediately precedes the read-out cycle and differs from the latter in only one respect, namely that the active word line is not shifted at all. The sense amplifier is activated in precisely the same time slot relative to the bit line voltage shifts as is the case in the subsequent read cycle. Thus, the cumulative charge detected during the pre-read cycle shall correspond very closely to the parasitic current contributions captured during the read cycle, including contributions from the active cell. The detected charge from the pre-read cycle is stored and subtracted from that recorded during the read cycle, yielding the desired net charge from the switching or non-switching transient in the active cell.

Clearly, the effects of fatigue, imprint, temperature and logic states are automatically taken care of by this referencing scheme. An important prerequisite is that the pre-read cycle must not materially alter the parasitic current levels in the read cycle. Thus, the delay between time points P6 and 0 (cf. Fig.14) must be sufficient for pre-read cycle transients to die down. In certain cases, two or more successive pre-read cycles may be employed to obtain a reproducible parasitic current response prior to the read cycle. However, this increases complexity and total readout time.

Inspection of Fig.14 in conjunction with the four level pulse protocol shown in Fig. 6 shows how the pre-read reference cycle principle may be implemented for the other pulse protocols covered by the present invention, by trivial extension of the example given in the present instance.

B.1.6. Switching protocols involving offset voltages.

Yet another scheme for circumventing or alleviating the problems relating to parasitic currents in non-addressed cells on active bit lines shall now be described.

According to Equation (2) above, the minimum disturbing voltage on non-addressed cells is $V_S/3$ (cf. Equation (3)) and the preferred embodiments described in conjunction with the 4- and 5 level switching protocols were shown to achieve this. As will be discussed below, it may in certain instances be preferable to deviate somewhat from this criterion.

Given that the memory cells exhibit certain characteristics regarding their electrical impedance and switching properties, it is possible to achieve a low parasitic current load on the bit line during read operations, while at the same time keeping disturbance of the non-addressed cells at a low level:

It is assumed that the selected cell is subjected to a voltage $V_i = V_S$ during the period when the memory material in the cell undergoes polarization switching. Thus,

$$(5) \qquad V_S = V_{ii} + V_{iii} - V_{iv} \ .$$

It is desired to lower the cumulative leakage current on the active bit line which flows through the non-addressed cells on that line. This can be achieved by lowering the voltage across the non-addressed cells by an amount δ. Thus,

$$(6) \qquad V_{iii} \rightarrow V_{iii} - \delta \ .$$

According to (5), this increment must be compensated by a corresponding adjustment in the voltages across the remaining non-addressed cells:

$$(7) \qquad V_{ii} - V_{iv} \rightarrow V_{ii} - V_{iv} + \delta \ .$$

In a large matrix, the number of cells with inactive word and inactive bit lines (V_{iv}) greatly outnumber the cells with an active word line crossing an inactive bit line (V_{ii}). To minimize the overall disturbance of non-addressed cells in the matrix, one may therefore impose the requirement that V_{iv} shall not be changed to compensate for the reduction in V_{iii} , in which case one has:

$$(8) \qquad V_{ii} \rightarrow V_{ii} + \delta \ .$$

Of course, this is not the only possible choice, but it shall be assumed hereafter to facilitate understanding of the basic principles involved.

Thus the $V_S/3$ protocol would be modified such that: $V_i = V_S$, $V_{ii} = V_S/3 + \delta$, $V_{iii} = V_S/3 - \delta$, $V_{iv} = -V_S/3$. This can be achieved by, e.g. leaving the potentials on the active word- and bit lines unchanged, while adding δ to all inactive word- and bit lines:

i) $V_i = V_S = \Phi_{activeBL} - \Phi_{activeWL}$: Active word line crossing active bit line (the selected cell)
ii) $V_{ii} = V_S/3 + \delta = (\Phi_{inactiveBL} + \delta) - \Phi_{activeWL}$: Active word line crossing inactive bit line,
iii) $V_{iii} = V_S/3 - \delta = \Phi_{activeBL} - (\Phi_{inactiveWL} + \delta)$: Inactive word line crossing active bit line,
iv) $V_{iv} = -V_S/3 = (\Phi_{inactiveBL} + \delta) - (\Phi_{inactiveWL} + \delta)$:Inactive word line crossing inactive bit line.

The magnitude of δ must be selected with due consideration to two conflicting requirements: On the one hand, it should be as large as possible in order to minimize parasitic current contributions to the active bit line. On the other hand, it should be as small as possible in order to minimize the disturbance of non-addressed cells. In practice, a decision must be made based on the specific conditions prevailing in each case.

EXAMPLE SHOWING HOW NON-LINEAR VOLTAGE-CURRENT RESPONSE IN NON-ADDRESSED CELLS MAKES THE ABOVE SCHEME WORK.

B.1.5. Full row readout.

An alternative route to reducing or eliminating the spurious current contributions from non-addressed cells along active bit lines during readout is illustrated in Fig.15: All word lines except the active one are clamped at a potential close to that at the sense amplifier input (defined as zero in Fig.15). For readout of data, the active word line is brought to the potential V_{READ}, which causes currents to flow through the cells on the crossing bit lines. The magnitudes of the currents depend on the polarization state in each cell and are determined by the sense amplifiers, one for each bit line as shown.

This scheme provides several advantages:
- Voltages across all non-addressed cells are very close to zero, eliminating leakage currents that may otherwise corrupt the readout from the addressed cells.
- The readout voltage V_{READ} may be chosen much higher than the coercive voltage without incurring partial switching in non-addressed cells. This allows for film switching speeds approaching the intrinsic switching speed of the polarizable material in the cells.
- The scheme is compatible with large matrix arrays.
- The high degree of parallelism makes possible a large data readout rate.

Since the readout is destructive, it shall in many cases be necessary to write data back into the memory device. This can be achieved by one of the pulsing schemes described in the previous paragraphs. A different set of cells in the memory device from those that were read may be chosen for refresh, e.g. in conjunction with caching.

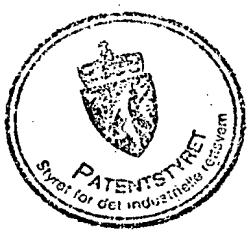
Possible disadvantages of this scheme are largely related to the increased demands on the circuitry performing the driving and sensing functions. Thus, the simultaneous switching of all cells on a long word line shall cause a large current surge on that line (implies a need for low source impedance in the driver stage and low impedance current paths. Also potential for cross-talk within the device). Furthermore, in order to avoid loss of data a separate sense

amplifier is needed on each bit line. With the highest possible density of cells in the passive matrix, this poses a crowding problem at the edge of the matrix where the sense amplifiers are connected.

B.1.6. Logic states.

The switching protocols described above make possible the controlled switching of polarization direction of any given cell in a passive matrix arrangement, without subjecting non-addressed cells to disturbing voltages that exceed $\approx V_s/3$.

As described in the examples above, the pulsing protocols are directly applicable to the reading of logic states in memory cells that either experience no polarization switching during the read cycle, defined as being in e.g. a logical "0", or switch the direction of the polarization, correspondingly defined as being in a logical "1". Initialization of the memory could involve the writing of 0's in all cells, which in the case above would imply performing a read pulse cycle (destructive read). Writing would then be achieved by applying the pulse sequence for changing the polarization in those cells that shall store a logical "1" while leaving the rest of the cells unchanged. Subsequent reading of data from the memory would then require a refresh cycle to be implemented in those cases where it is desired to retain data in the memory following the destructive read. The refresh protocol would require a complete read/refresh pulse sequence in cases where other cells are used for renewed storage than those that were read destructively to provide the data. On the other hand, if the same cells are used, those cells that were read as logical "0" can be left unchanged and only those that contained a "1" need to be exposed to polarization switching.



C. Patent claims.

1. A method of driving a passive matrix addressed display or memory array of cells containing an electrically polarizable material exhibiting hysteresis, in particular a ferroelectric material, whereby the polarization state in individual, separately selectable cells can be switched to a desired condition by application of voltages to the word- and bit lines in said matrix,
   c h a r a c t e r i z e d b y
   - controlling individually the potential on selected word- and bit lines to approach or coincide with one of n predefined potential levels, where $n \geq 3$, the potentials on said selected word- and bit lines forming subsets of said n potentials involving n_{WORD} and n_{BIT} potentials, respectively,
   - controlling the potentials on all word- and bit lines in time in a coordinated fashion according to a protocol or timing sequence whereby wordline potentials are latched in a predetermined sequence to potentials selected among the n_{WORD} potentials, while bit lines

- are either latched in a predetermined sequence to potentials selected among the n_{BIT} potentials or they are during a certain period of the timing sequence connected to circuitry that senses the charges flowing between the bit line(s) and the cells connecting to said bit line(s),
- arranging said timing sequence to encompass at least two distinct parts, including a "read cycle" where charges flowing between said selected bit line(s) and the cells connecting to said bit line(s) are sensed, and a "refresh/write cycle" where polarization state(s) in cells connecting with selected word- and bit lines are brought to correspond with a set of predetermined values.

2. As Claim 1,
characterized by
allowing one or more bit lines to float in response to charges flowing between the bit line and the cells connecting to said bit line during said read cycle, and clamping all voltages on the word- and bit lines during the refresh/write cycle.

3. As Claim 1 or 2,
characterized by
selecting the values $n = 3$ and $n_{WORD} = 3$ and $n_{BIT} = 3$, and where the voltages across non-addressed cells do not significantly exceed $V_S/2$, where V_S is the voltage across the addressed cell during read, refresh and write cycles

4. As Claim 1 or 2,
characterized by
selecting $n = 4$ and $n_{WORD} = 4$ and $n_{BIT} = 4$, and where the voltages across non-addressed cells do not significantly exceed $V_S/3$, where V_S is the voltage across the addressed cell during read, refresh and write cycles

5. As Claim 1 or 2,
characterized by
selecting $n = 5$ and $n_{WORD} = 3$ and $n_{BIT} = 3$, and where the voltages across non-addressed cells do not significantly exceed $V_S/3$, where V_S is the voltage across the addressed cell during read, refresh and write cycles

6. As one or more of the foregoing claims,
characterized by
subjecting non-addressed cells along an active word line and along active bit line(s) to a maximum voltage during the read/write cycle that deviates by a controlled value from the exact values $V_S/2$ or $V_S/3$.

7. As Claim 6,
characterized by
subjecting non-addressed cells along an active word line to a voltage of a magnitude that exceeds the exact values $V_S/2$ or $V_S/3$ by a controlled voltage increment, and at the same time subjecting non-addressed cells along selected active bit lines to a voltage of a

magnitude that is less than the exact values $V_S/2$ or $V_S/3$ by a controlled voltage decrement.

8. As Claim 6 or 7,
characterized by
the controlled voltage increment and voltage decrement being equal to each other.

9. As Claim 6, 7 or 8,
characterized by
adding a controlled voltage increment δ_1 to the potentials $\Phi_{inactiveWL}$ of inactive word lines and adding a controlled voltage increment δ_2 to the potentials $\Phi_{inactiveBL}$ of inactive bit lines, where $\delta_1 = \delta_2 = 0$ corresponds to the read/write protocols with maximum $V_S/2$ or $V_S/3$ voltage exposure on non-selected cells.

10. As Claim 9,
characterized by
$\delta_1 = \delta_2 \neq 0$.

11. As one or more of the preceding claims,
characterized by
controlling the quiescent potential (the potential imposed on the word- and bit lines during the time between each time the read/refresh/write cycle protocol is employed) to have the same value on all word- and bit lines, i.e. a zero voltage is imposed on all cells.

12. As one or more of the preceding claims,
characterized by
selecting the quiescent potentials on one or more of the word- and bit lines among one of the following: a) System ground, b) Addressed word line at initiation of pulsing protocol, c) Addressed bit line at initiation of pulsing protocol, d) Power supply voltage (V_{CC}).

13. As one or more of the preceding claims,
characterized by
selecting the potential on the selected bit line(s) in the quiescent state such that it differs from that at the onset of the floating period (read cycle), and by said potential being brought from the quiescent value to that at the onset of the floating period, where it is clamped for a period of time comparable to or exceeding the time constant for charging the bit line ("pre-charge pulse").

14. As one or more of the preceding claims,
characterized by
preceding the reading cycle with a voltage shift on the inactive word lines, whereby the non-addressed cells on the active bit line are subjected to a voltage bias equal to that ocurring due to the active bit line voltage shift during the read cycle, said voltage shift on the inactive word lines starting at a selected time preceding said voltage shift on the active bit line, and terminating at the time when the latter voltage shift is initiated, in such a way

that the perceived voltage bias on said non-addressed cells on the active bit line is continuously applied from the time of initiation of said voltage shift on the inactive word lines and up to the time of termination of said voltage shift on the active bit lines ("pre-charge pulse").

15. As one or more of the preceding claims,
characterized by
applying a pre-read reference cycle which precedes the read cycle and is separated from it by a selected time, and which mimics precisely the pulse protocol and current detection of said read cycle, with the exception that no voltage shift is imposed on the active word line during said pre-read reference cycle, and by emloying the recorded signal during said pre-read reference cycle as input data to the circuitry that determines the logic state of the addressed cell.

16. As claim 15,
characterized by
said recorded signal during the pre-read cycle being subtracted from the recorded signal during the read cycle.

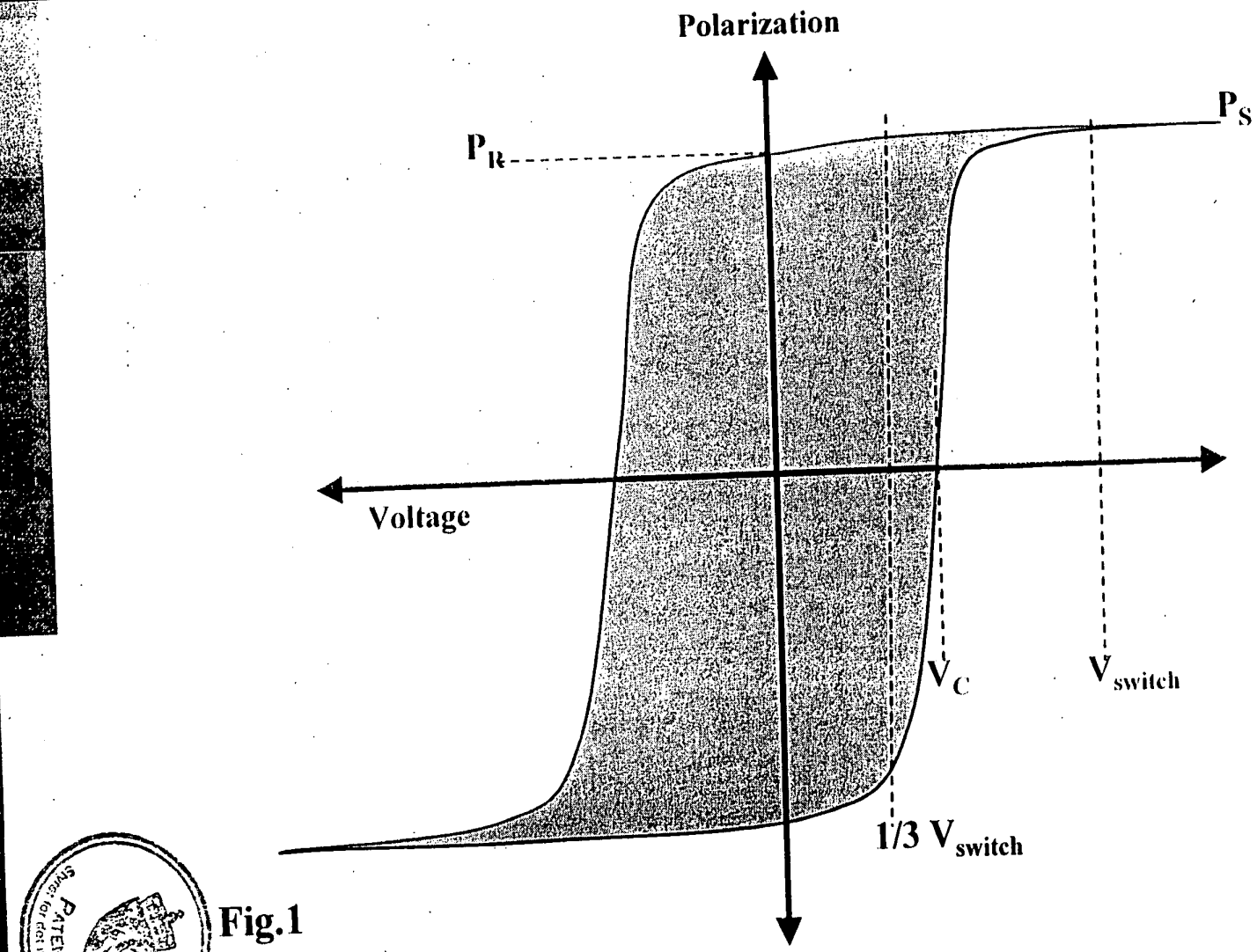


Fig.1

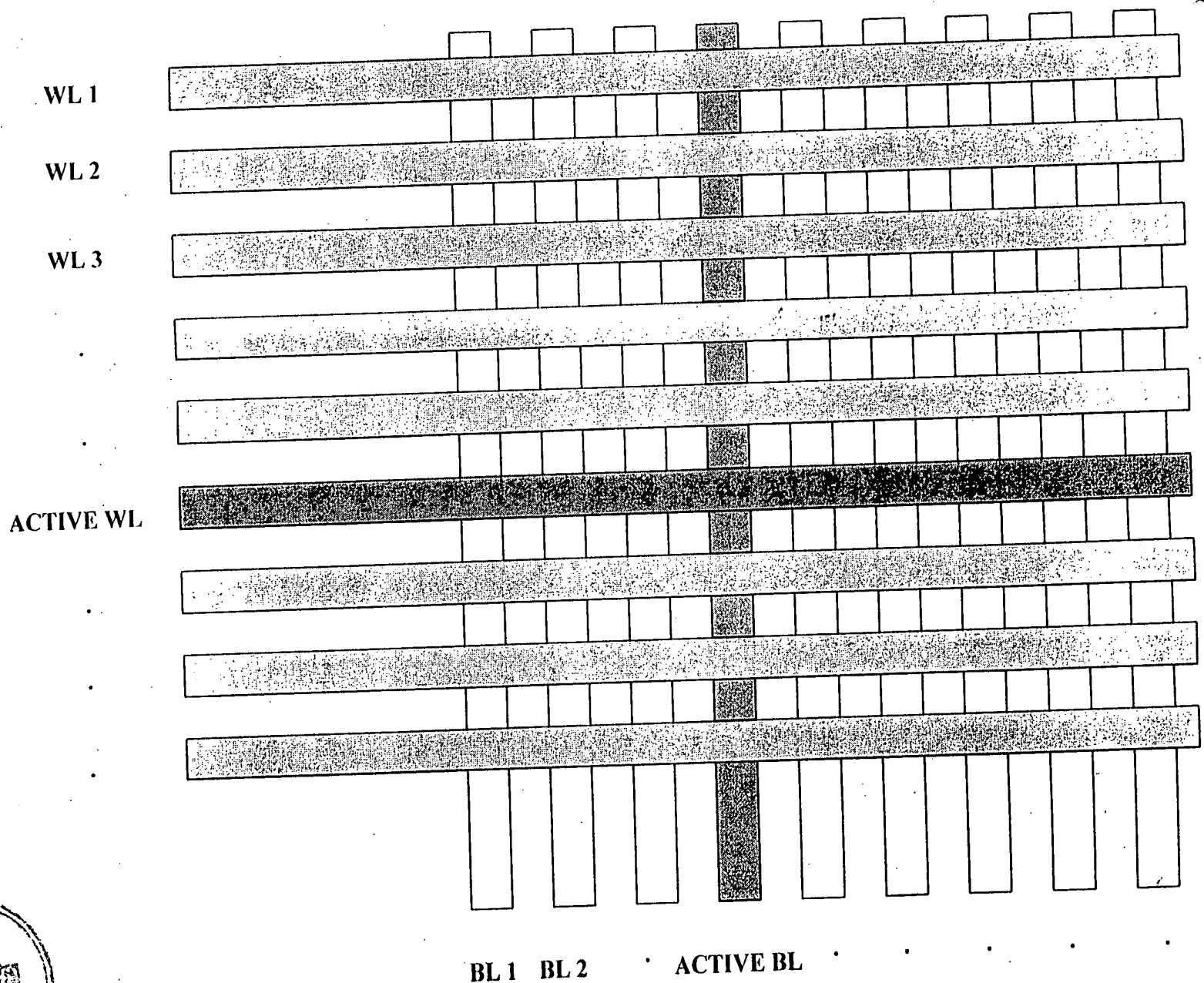


FIG.2

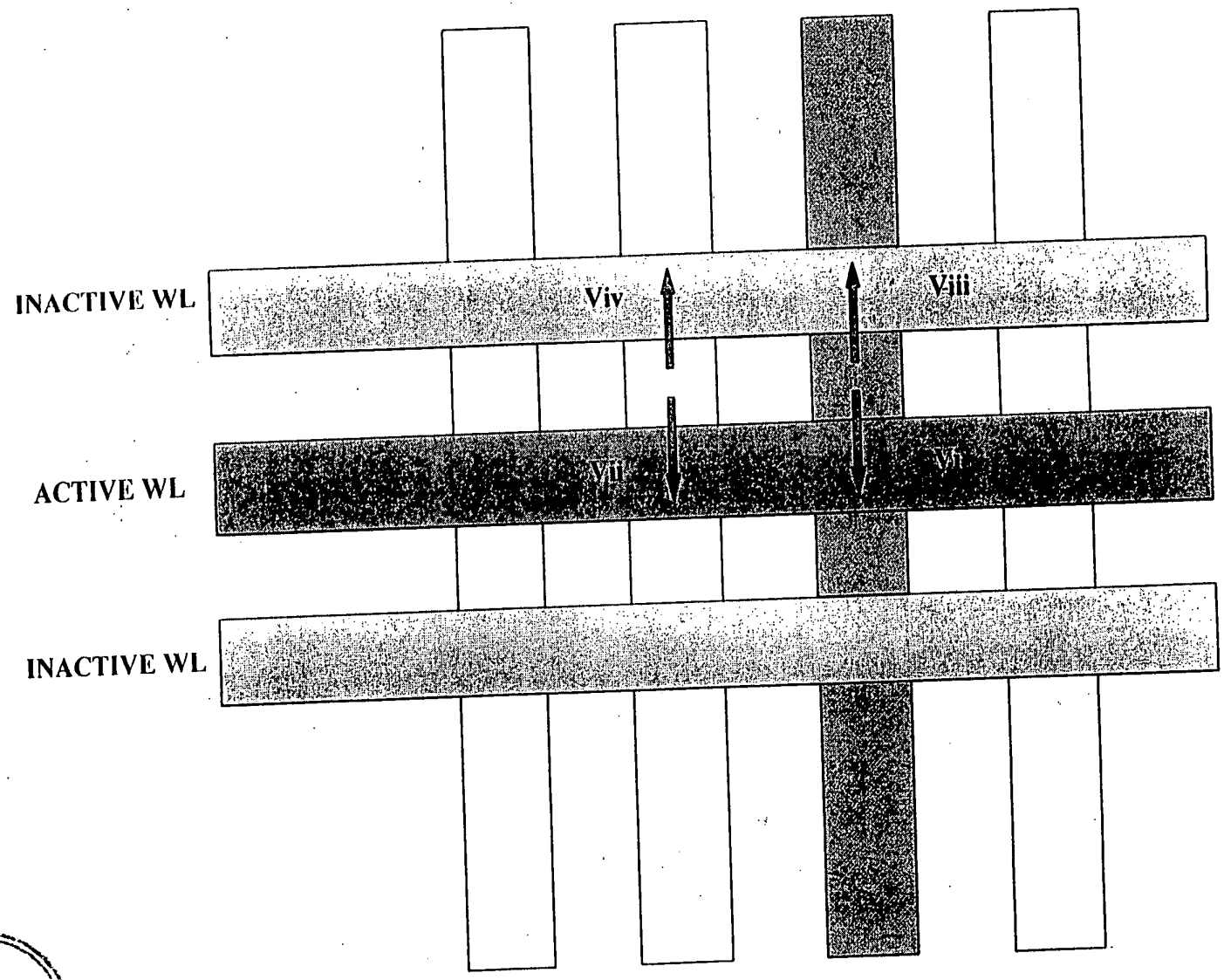
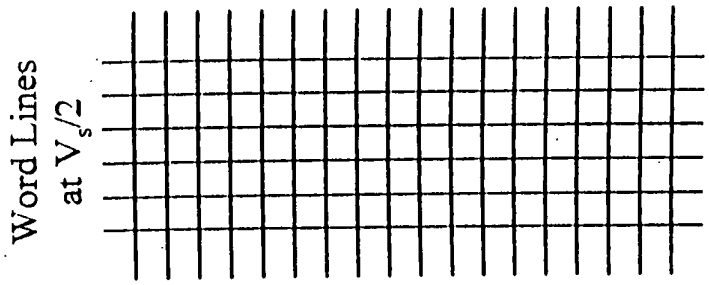

INACTIVE WL
ACTIVE WL
INACTIVE WL
Viv
Viii
Vii
Vi
INACTIVE BL
INACTIVE BL
ACTIVE BL
INACTIVE BL

FIG.3

3 *Level Passive Matrix Switching Protocol*

- t_0: word line latched, active pulldown to 0
- t_1: bit line clamp released - sense amp on
- t_2: bit line decision - data latched
- t_3: word line returned to quiescent $V_s/2$
- t_4: write data latched on bit lines
- t_5: word line pulled to V_s - set/reset caps
- t_6: word line returned to quiescent $V_s/2$
- t_7: bit lines actively returned to V_s clamp
- t_8: read/write cycle complete

Maximum depolarizing voltage Vs/2



Sense Amps biased near V_s

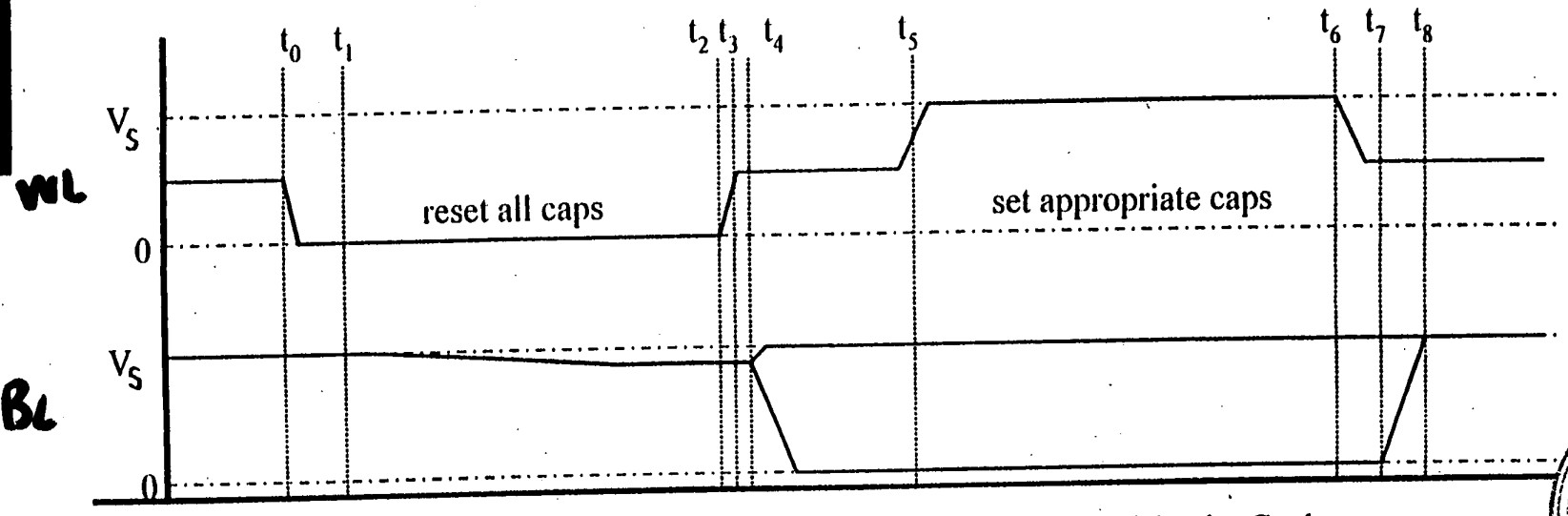
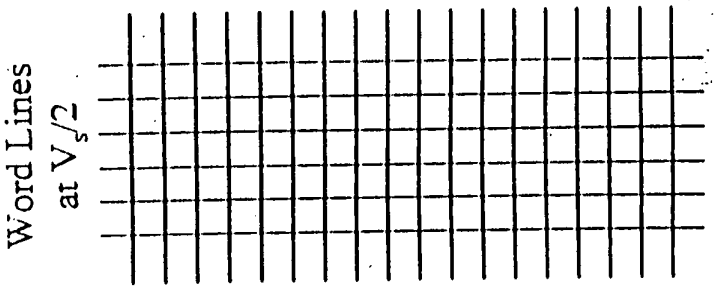


FIG. 4

3 *Level Passive Matrix Switching Protocol*

- t_0: word line latched, active pull up to V_s
- t_1: bit line clamp released - sense amp on
- t_2: bit line decision - data latched
- t_3: word line returned to quiescent $V_s/2$
- t_4: write data latched on bit lines
- t_5: word line pulled to 0 - set/reset caps
- t_6: word line returned to quiescent $V_s/2$
- t_7: bit lines actively returned to 0 clamp
- t_8: read/write cycle complete

Maximum depolarizing voltage Vs/2



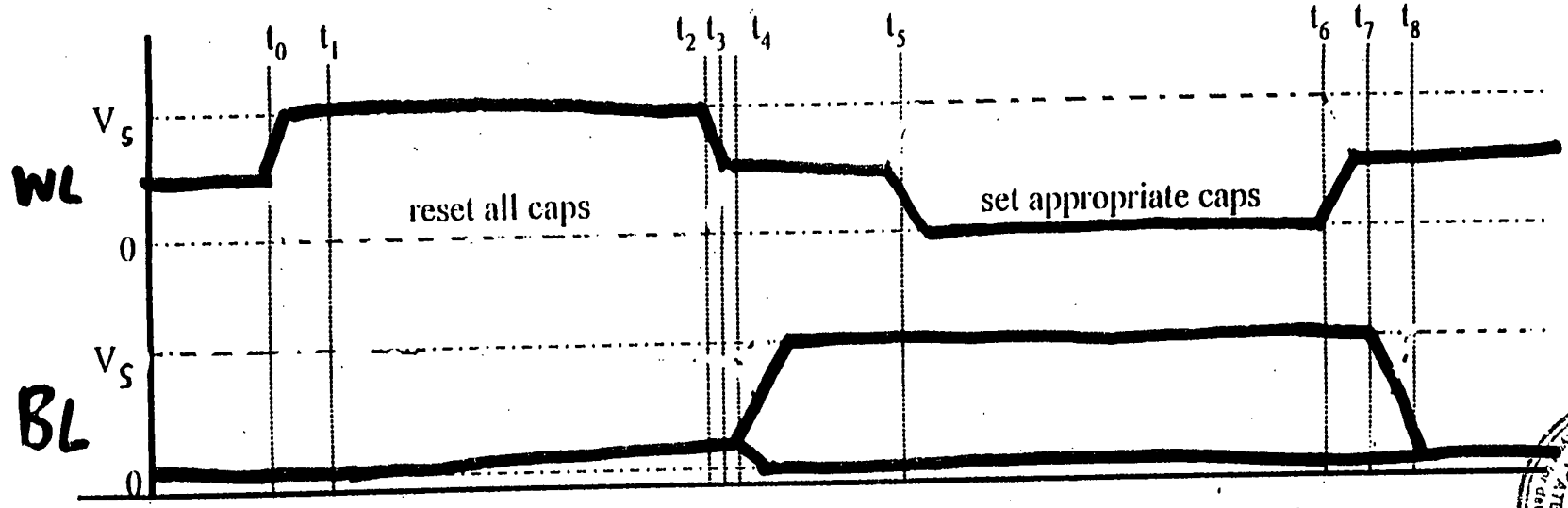


FIG. 5

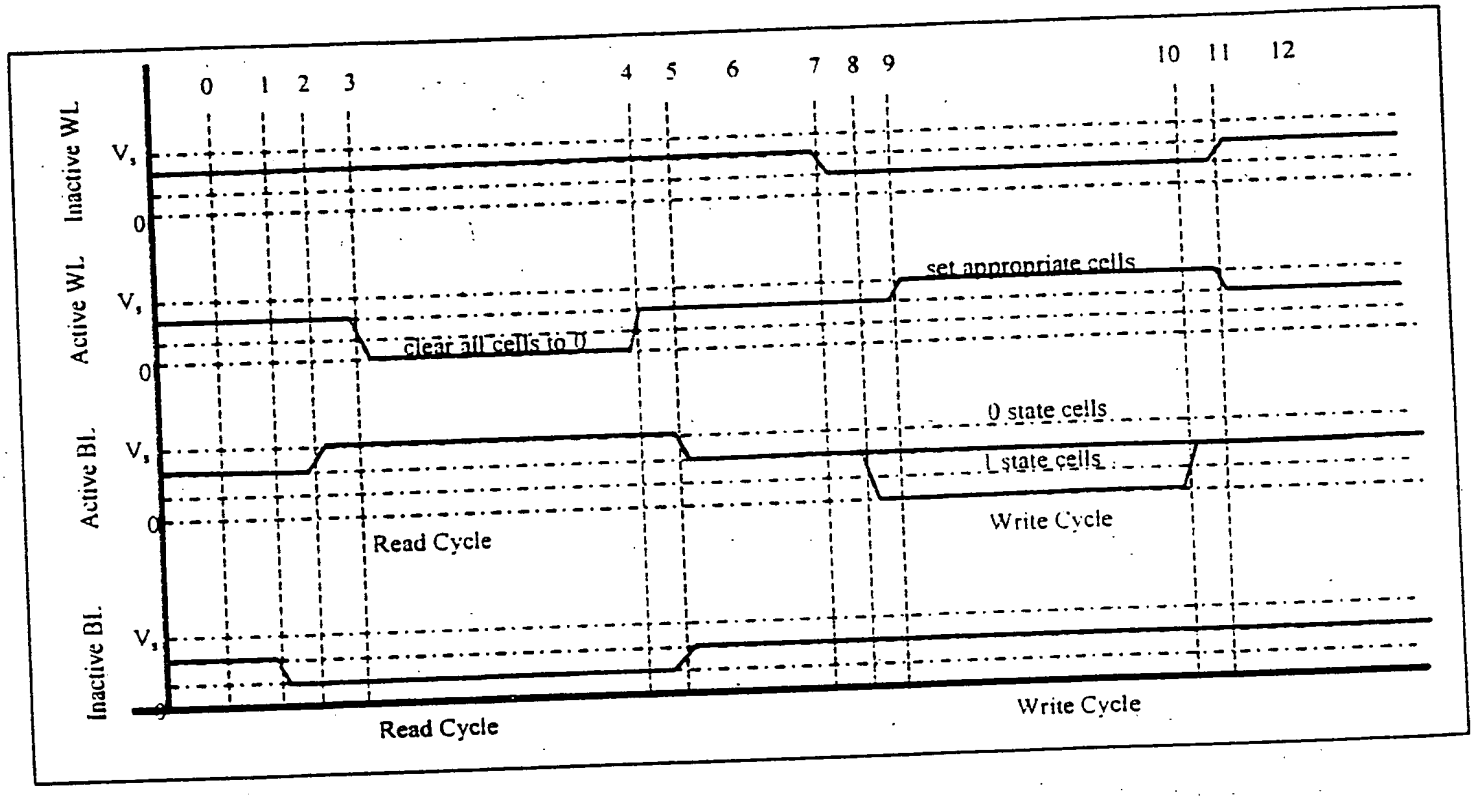


FIG. 6.

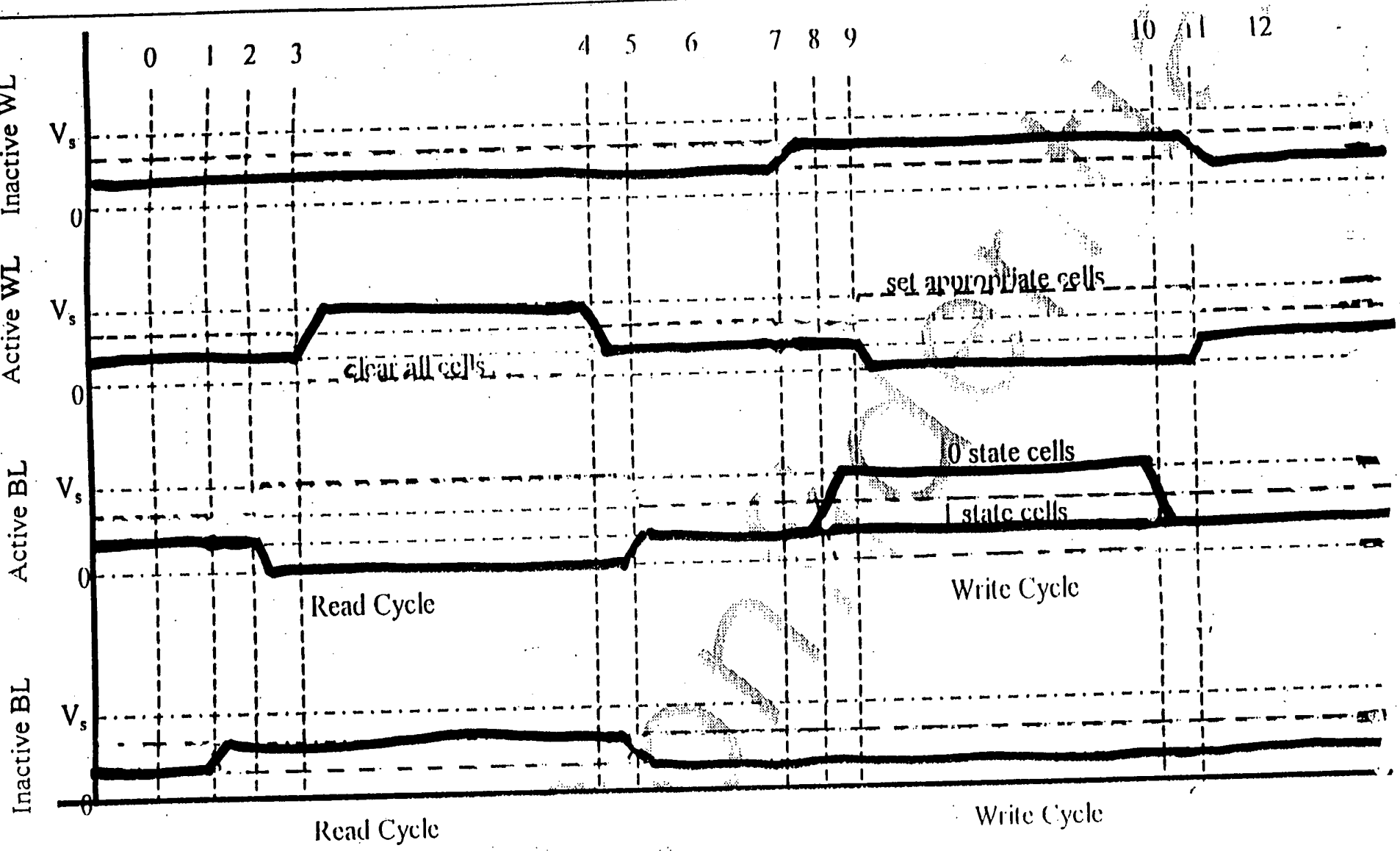

0
1
2
3
4
5
6
7
8
9
10
11
12
Inactive WL
Active WL
Active BL
Inactive BL
V_s
0
clear all cells
set appropriate cells
0 state cells
1 state cells
Read Cycle
Write Cycle
Read Cycle
Write Cycle

FIG. 7

Five Level Timing Diagram

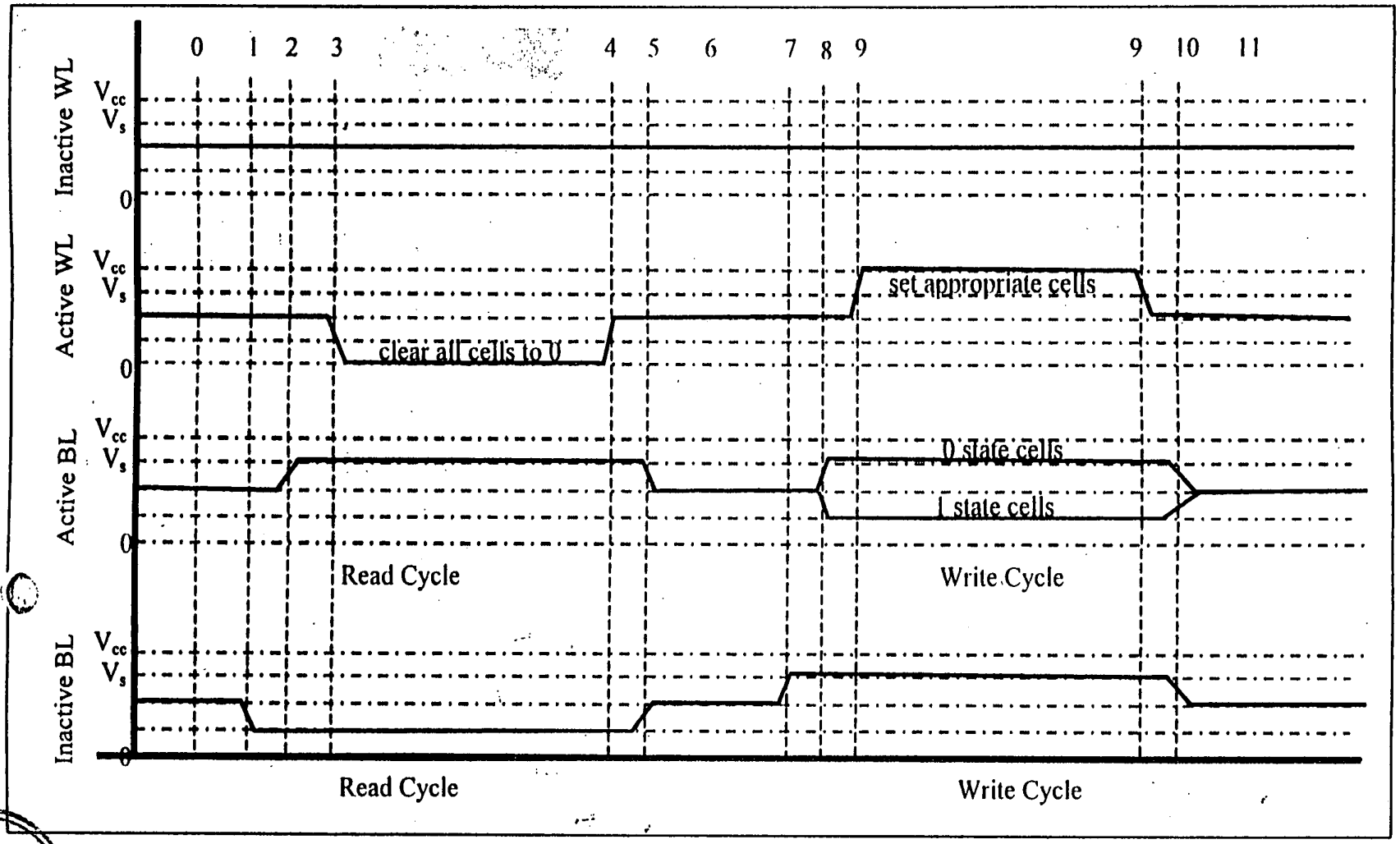


FIG. 8

Five Level Timing Diagram

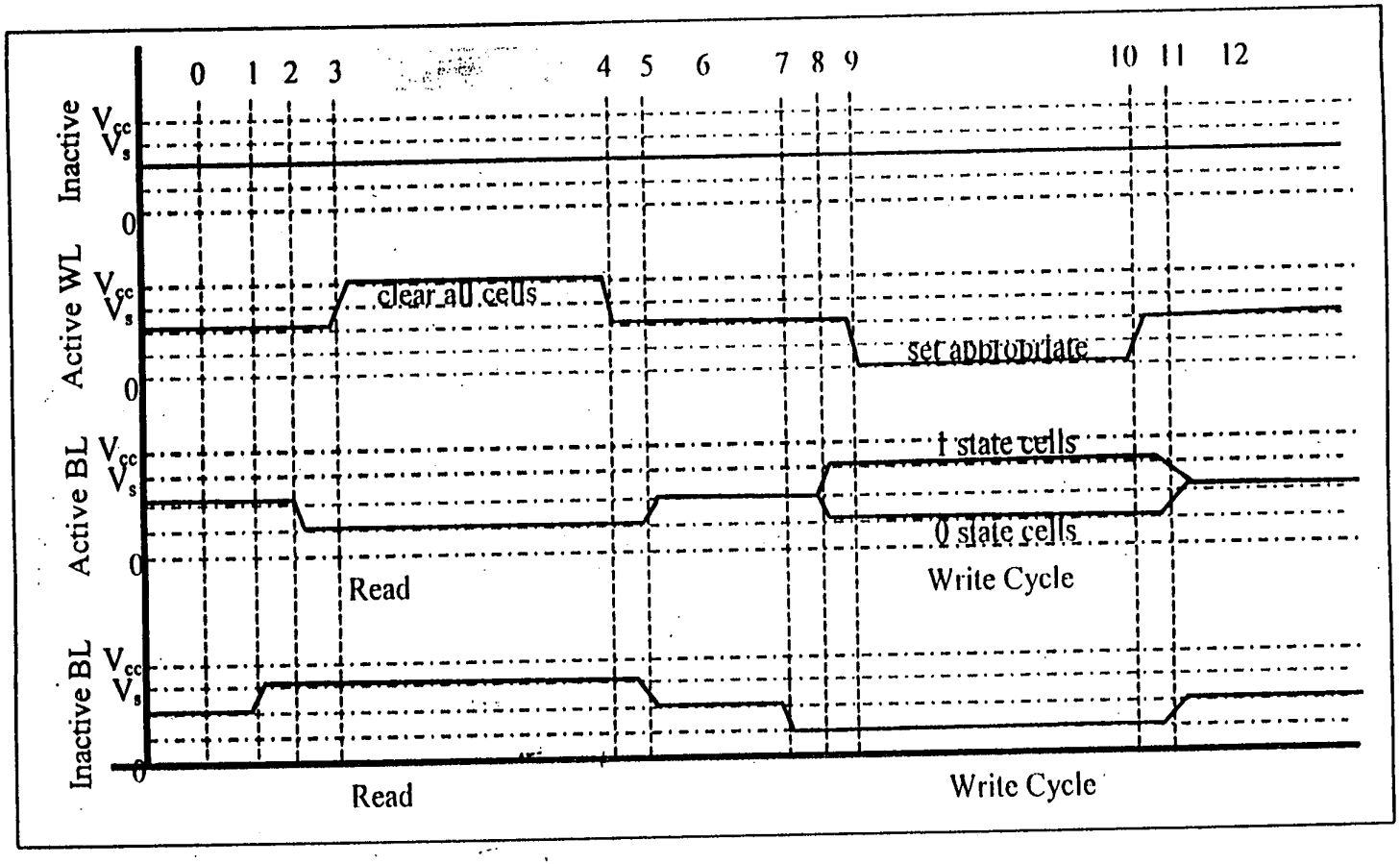


FIG. 9

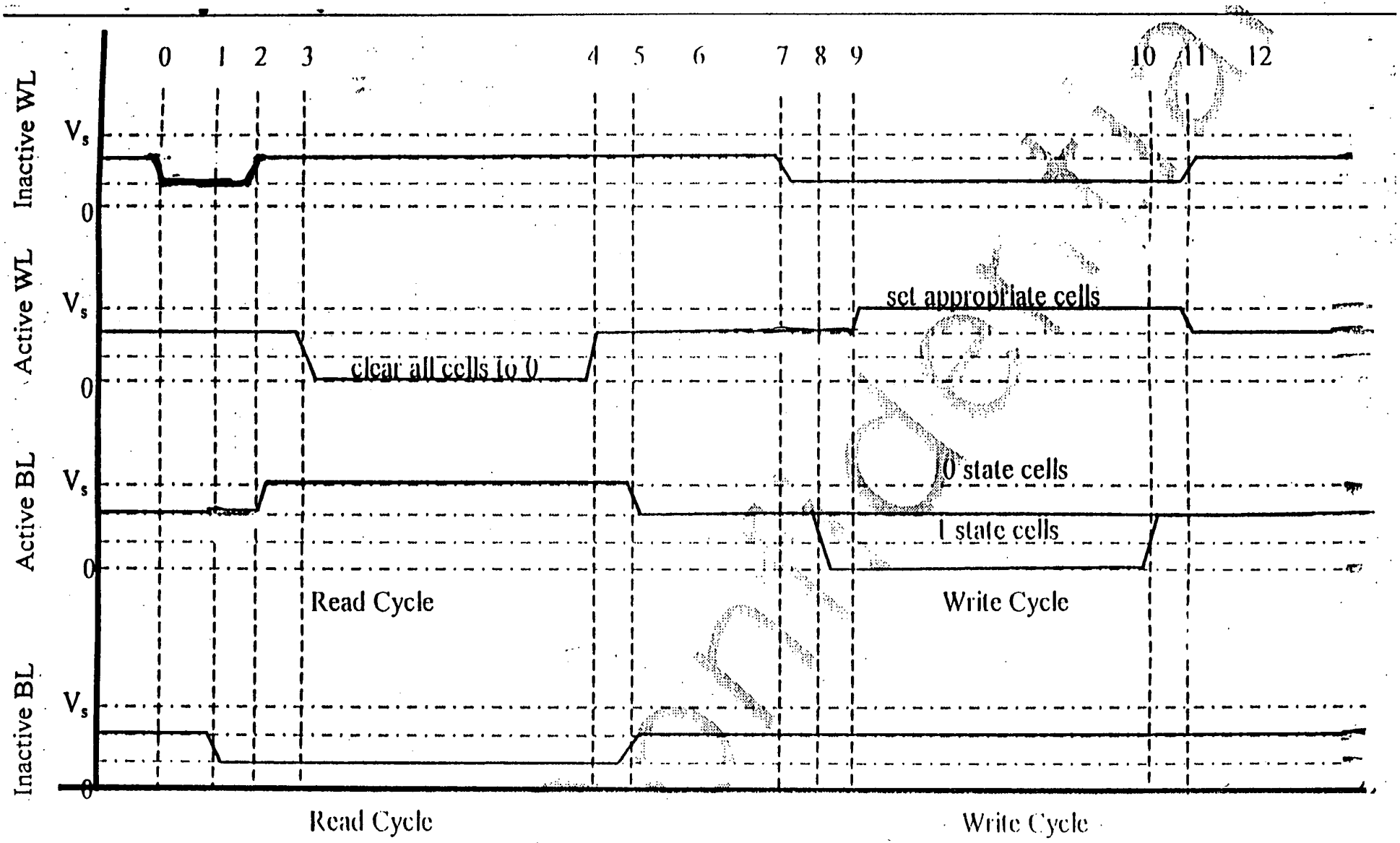

0
1
2
3
4
5
6
7
8
9
10
11
12
Inactive WL
Active WL
Active BL
Inactive BL
Vs
0
clear all cells to 0
set appropriate cells
0 state cells
1 state cells
Read Cycle
Write Cycle
Read Cycle
Write Cycle

FIG. 10

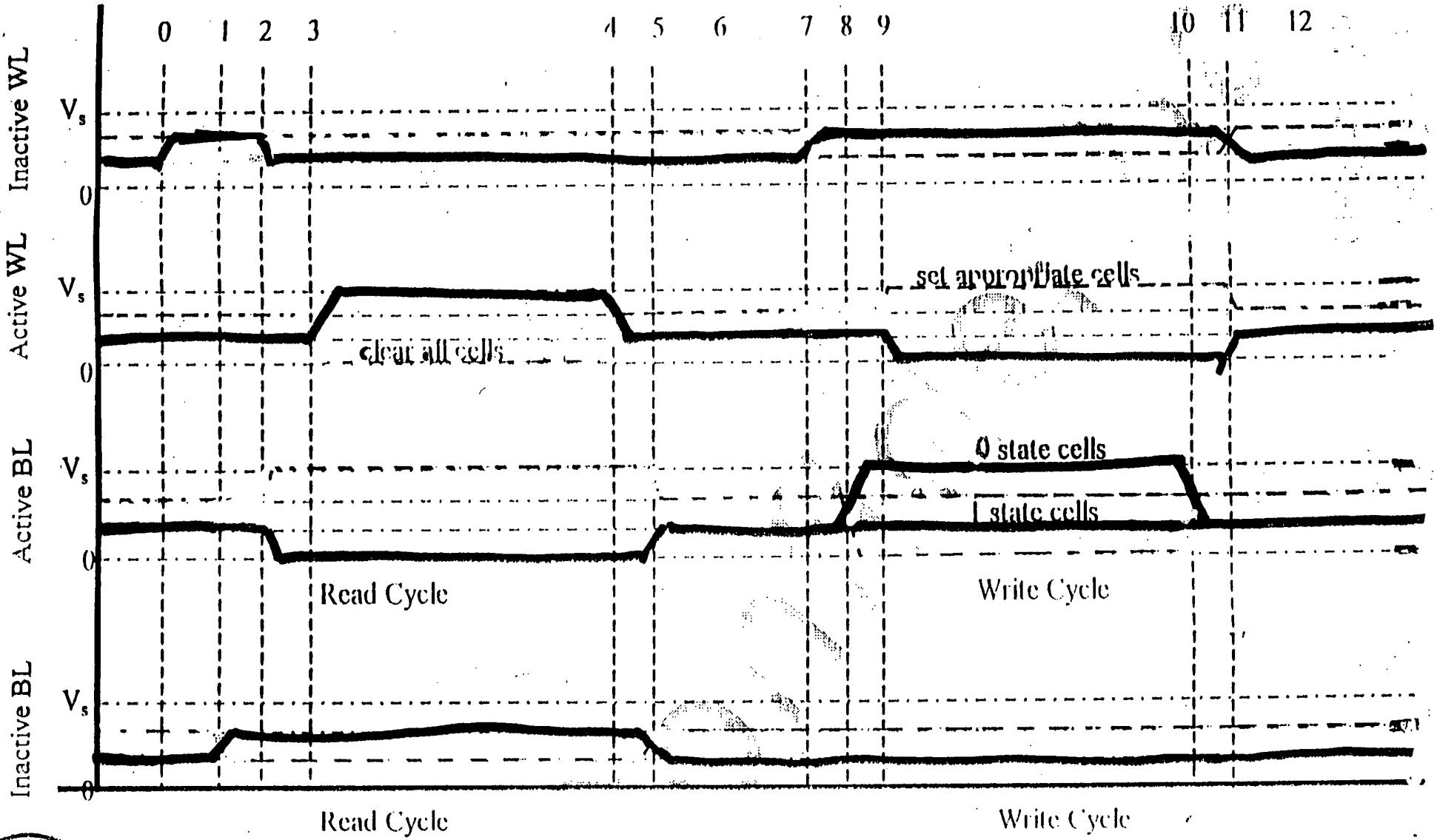

0
1
2
3
4
5
6
7
8
9
10
11
12
Inactive WL
Active WL
Active BL
Inactive BL
V_s
0
clear all cells
set appropriate cells
0 state cells
1 state cells
Read Cycle
Write Cycle
Read Cycle
Write Cycle

FIG. 11

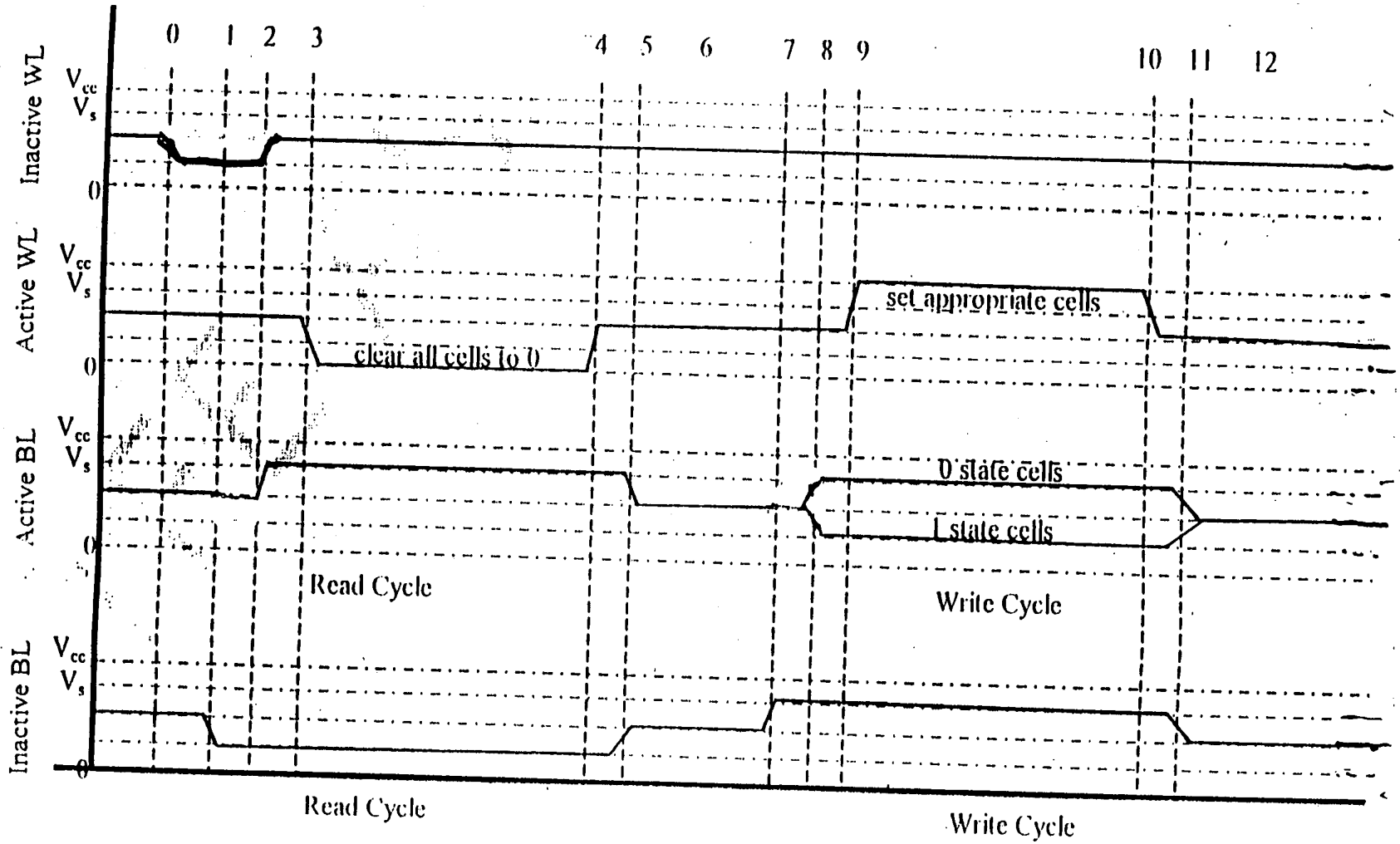


FIG.12

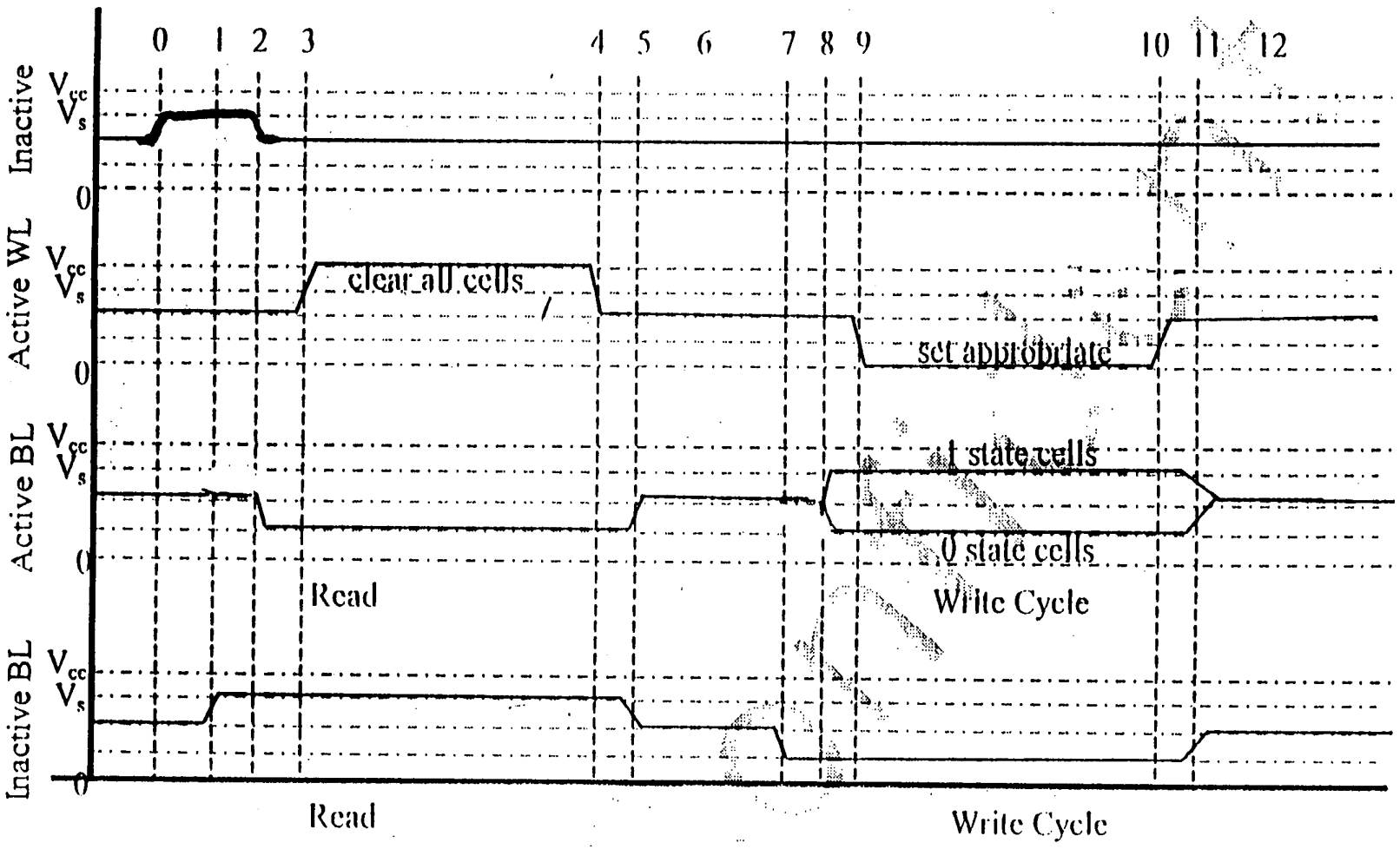


FIG. 13

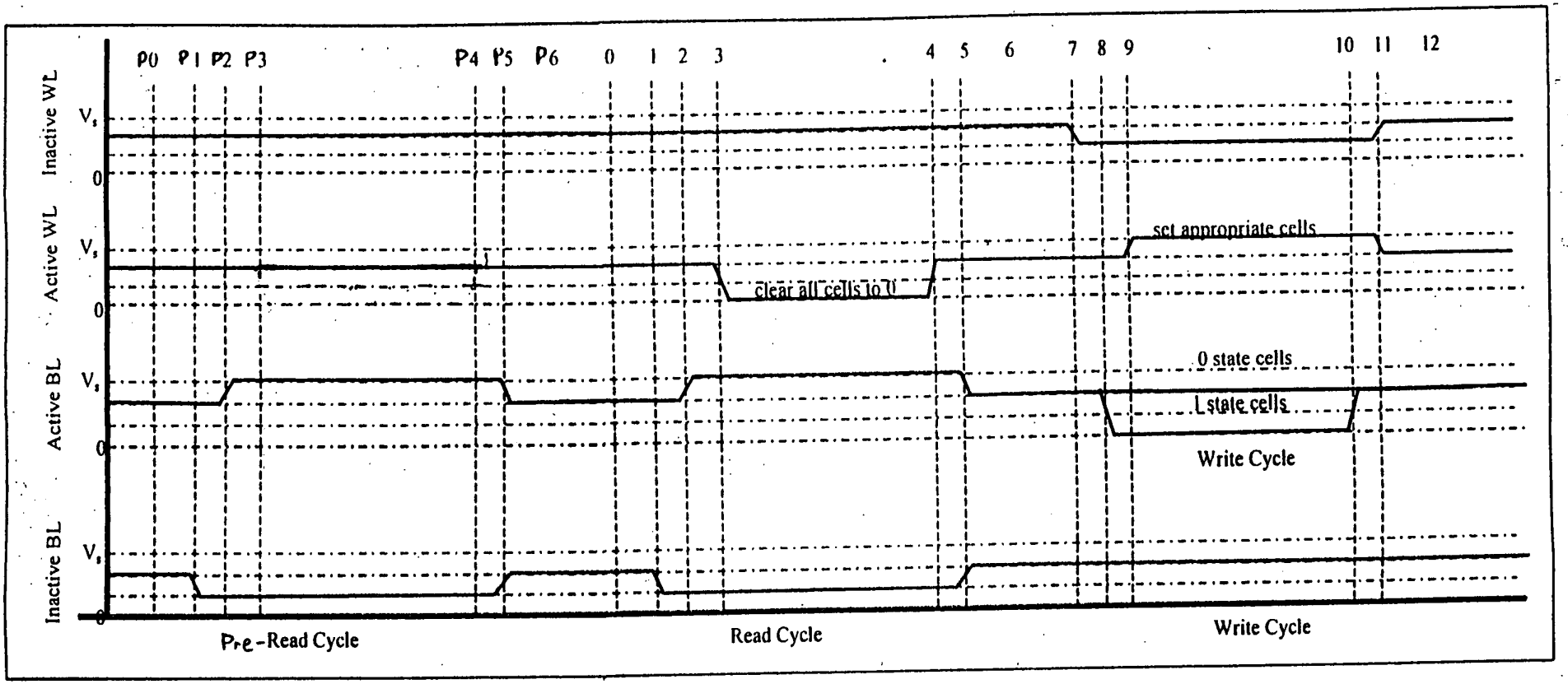


FIG. 14

EXAMPLE OF READ AND WRITE PROTOCOL INVOLVING A PRE-READ REFERENCE CYCLE.

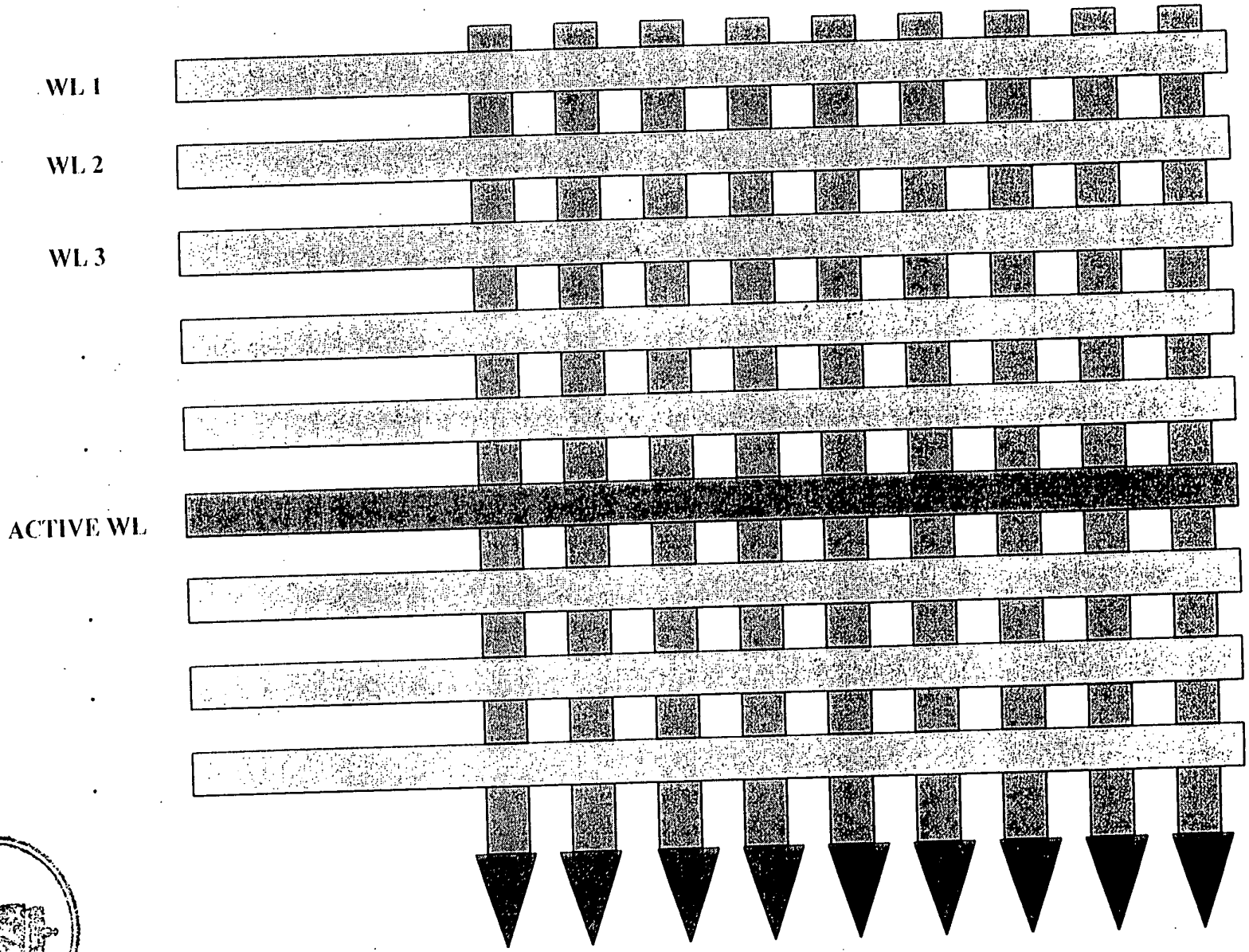


FIG.15